A Fully Packaged 4x4 Integrated Optical Switch Matrix

Riccardo Varrazza [a], Terry Bricheno [b], and Siyuan Yu [a], *member IEEE*

Abstract — **This paper describes a packaged and fibre array coupled 4x4 optical crosspoint switch designed for optical packet switching. Alignment and fixation techniques of two perpendicular fibre arrays to the integrated InP based switch chip has been developed. Thermal management is also included in the packaging. The packaged devices demonstrate long term stability and have been used in switch modules including the packaged device and electronic interfaces.**

Index Terms— **Optoelectronic device Packaging, Micro-Optics, Optical cross-connect, integrated optoelectronics, optical crosspoint switch, optical packet switching, Optical Multicast Switching.**

1 INTRODUCTION

One of the most important elements in future optical packet switching networks is an optical crosspoint switch (OXS). It is a component able to route optical packets [1-6] within few nanoseconds [7] with high extinction ratio, low polarization dependent loss, low loss and good port count scalability.

Over recent years we have developed an optical crosspoint switch (OXS) technology [8] that is promising high performance for optical packet switching (OPS) operations [9]. A typical device is a 4x4 switch matrix integrated on InP substrate using active vertical coupler (AVC) structures. With this kind of device we have demonstrated several desirable functions such as OPS, OPS and simultaneous wavelength conversion [10], label recognition and optically addressed packet switching [11], and lossless optical multicasting [12].

In order to apply the device in real networking applications, packaged devices and switch modules need to be developed. A key problem in the packaging process is to develop feasible fibre coupling strategies. Reducing the packaging cost is also an important design optimization consideration. This relies on an optimised fibre alignment strategy together with the adoption of cheaper materials, simplifying the assembly processes, and using components that can be potentially out-sourced.

This paper is divided into three main sections. Section 2 describes the OXS chip includes working principles and structural as well as operational characteristics which pre-determine to a large extent how the package should be designed. Section 3 describes the packaging design and implementation process of the OXS, discussing the important parts and issues involved. Section 4 present test results.

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a) Department of Electrical & Electronic Engineering, University of Bristol, Bristol BS8 1UB, United Kingdom. (e-mail: R.Varrazza@bristol.ac.uk)
b) Afonics, 16 Thorney Leys Business Park, Witney, Oxfordshire. OX28 4GW

2 THE OPTICAL CROSSPOINT SWITCH CHIP

The switch matrix to be packaged is integrated on InP substrates, consisting of 16 interconnected optical switch cells. Each single cell involves two passive waveguides crossing each other at 90° angle. The passive waveguide are made of wider bandgap material and have low loss at the operating wavelength of 1550nm. These passive waveguides form the signal input and output. Two active vertical couplers (AVC) are realised at the crosspoint by stacking on top of each passive waveguides an active waveguide layer. For 'active' we mean that the waveguides have either significant loss or gain to the optical signal concerned, and that the gain/loss and refractive index can be modulated by current injection. A total internal reflection (TIR) mirror cuts vertically through the active waveguides and diagonally across the waveguides intersection allowing the 90° redirection of the optical signal.

This structure allows switching by simultaneous refractive index and gain/absorption modulation. By carrier injection, the refractive index of the active upper waveguide is reduced to match that of the lower waveguide to allow coupling. Thus, when in the ON state, the optical signal present at input passive waveguide is coupled up to the active waveguide in the first AVC, turned by 90° at the TIR mirror, and then coupled down in the second AVC, to the output passive waveguide. When in OFF state no carriers are injected so the optical signal does not interact with the active layer and travels straight through to next switch cell. Any residual coupling into the active layer is absorbed by its high loss therefore little leakage should appear at the output.

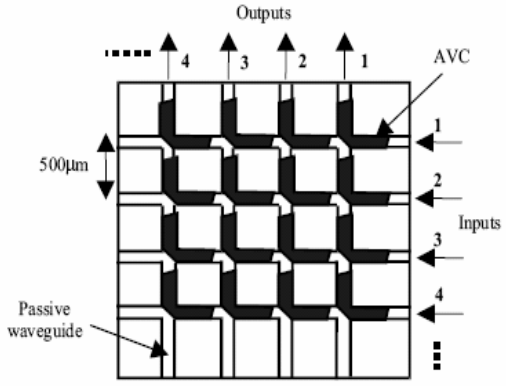


Fig.1 Optical Switch Cell Employing an Active Switching Mechanism and Passive Waveguide Signal Paths

When operated in a point-point switching application, up to 4 input signals can be simultaneous switched through the matrix if they do not content with each other. Upper level control circuits will turn 'ON' four switch cell which will redirect the optical signals to their intended output. Referring to Fig.1, for example with input 4 to be switched to output 3, the first 2 cell in the same (4^{th}) row are in OFF state allowing the signal to travel up to the third cell where it is switched to the output 3 after passing through all other cells in the 3^{rd} column which are also in OFF state. Therefore, as a rule, no more than one switch is switched on in any row or column, and the maximum number of cells switched on simultaneously will be ≤4.

All the waveguide layers are MOVPE grown on InP. The designed structure has an intrinsic separate confinement heterostructure (SCH) active waveguide with 7x75Å unstrained InGaAs QWs (λ_{PL}=1560nm) separated by 60Å Q1.3 barriers. The Q1.2 passive waveguide layer is 0.7μm thick and the spacing layer between the active layer and the passive waveguide layer is 1.35μm thick. The wafer is processed into 4x4 switch matrices with 500x500μm^2 switch cell size, 450 μm AVC length and 5 μm waveguide width.

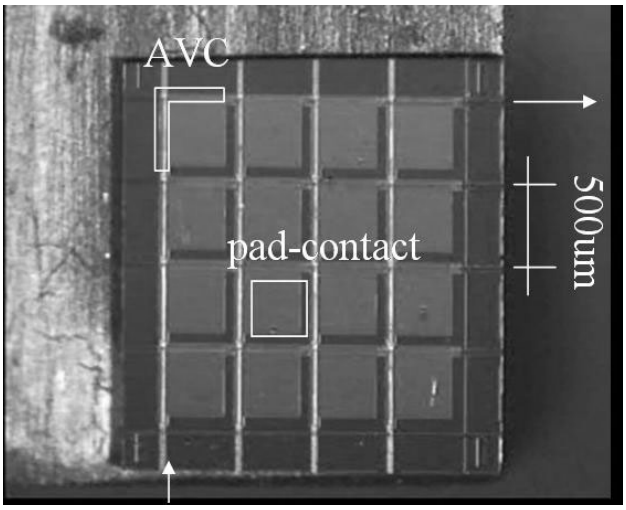


Fig. 2 A cleaved 4x4 OXS Matrix

A finished 4x4matrix is shown in Fig.2. The cleaved switch matrix chips are 2.5×2.5 mm^2 in size, and are anti-reflective (AR) coated on all 4 facets to <1x10^{-3} reflectivity using a single layer dielectric film.

3 PACKAGING

3.1 Overall design

The unique structure of this photonic component require a special package with 22 electrical connections and 2 fibre array pigtails each containing 4 fibres which need to be coupled to the chip with minimum optical coupling loss. The chip is an active device which will generate heat. This heat needs to be effective removed so that the temperature of the chip can be kept at suitable levels in a range of environment temperatures.

Fig. 3 schematically illustrates the component needed inside the package case. A thermo-electrical cooler (TEC) is used to transport the heat generated by the device. The large number (16) of electrical connection to the chip needs to be fanned out to allow connection to outside the case via feed through pins. A thermistor as the temperature sensor is also needed. A critical consideration in designing the packaging structure is that the two fibre ribbons and the chip itself need to be supported stably by a common platform, which is free from thermal expansions. This would be best satisfied by a design in which the common support for the chip and the fibre ribbon is temperature controlled. In our design this is provided by the electrical fan-out submount which is to be bonded to the top ceramic surface (cold side) of the TEC, and the entire submount is temperature controlled by the TEC.

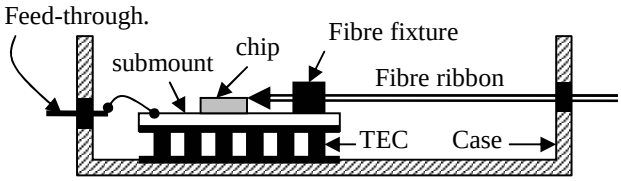


Fig.3 A sketch of the package

3.2 Thermal Management

The choice for the TEC is determined by the size of the submount and by the amount of heat to be pumped off.

A proper thermal analysis considering the heat load allows a better cooling efficiency and reduced power consumption. The heath load estimation is based on active heath load and passive characteristics such as radiation, convection, and conduction.

Active Heat Load

The active heat load is the heat generated by the switch chip, and can be calculated using the formula:

$$Q_{active} = 4VI \qquad (1)$$

where $\mathbf{Q_{active}}$ is the active heat load in *watts* ,**V** is the voltage (in Volts) across the switch cell and **I** the injected current (in Amps) through the device. The factor of 4 is due to the operational mode of the OXS device in which the number of cells simultaneous in ON state is at most 4. From previous test data the maximum switching current is about 300mA per switch cell. At the current the maximum device voltage is about 1.5V, therefore the active heat load is 1.8W.

Radiation

Radiation heath exchanged between two objects at different temperature is expressed by the formula

$$Q_{rad} = FesA\left(T_{amb}^4 - T_c^4\right) \qquad (2)$$

where: $\mathbf{Q_{rad}}$ is the radiation heat load in *watts*. **F** is called shape factor while **e** is the emissivity, both assume values between 0 and 1 with the latter representing the worst case. **s** is the Stefan-Boltzman costant and **A** represent the area of the cooled surface in m^2. Finally the two temperatures are: T_{amb}, ambient temperature and T_c temperature at the cold ceramic side of the TEC. Both temperature are expressed in *Kelvin*.

Thus in our case assuming the worst cases for both shape factor and emissivity, an area of 6.25x10^{-6} m^2, T_c ~ 17°C, and considering two different ambient temperatures of respectively 70 and 50°C, Q_{rad} is in the range 0.00135 to 0.00240 W.

Convection

Convective heath load is due to the difference of temperature between the surrounding air (or fill gas) and the component. It is a natural effect when the package does not include forced ventilation. Clearly the effect is related to the area in strict contact with the gas. The fundamental equation describing the effect is:

$$Q_{conv} = hA\left(T_{gas} - T_c\right) \qquad (3)$$

where $\mathbf{Q}_{conv}$ is the convective heath load in watts, **h** convective heath transfer coefficient expressed in w/m^2C. A typical value of **h** is 21.7 for a flat, horizontal plate in air at the pressure of 1 atmospheric pressure. **A** is the area in m^2 while $\mathbf{T}_{gas}$ and $\mathbf{T}_c$, both expressed in degree Celsius, representing respectively the temperature of the surrounding gas and the temperature at the cold ceramic side of the TEC. In our design the total Q_{conv} is about 0.00448 W

Conduction

Conductive heat transfer occurs when energy exchange takes place by direct impact of molecules from a high temperature region to a low temperature region. Conductive heat loading on a system may occur through lead wires, mounting screws, etc., which form a thermal path from the device being cooled to the heat sink or ambient environment.

In our design the only possible conduction paths in contact with the cold side of the TEC are gold bonding wires between the fan-out submount and the package feed-through pins. These gold wires are 50μm in diameter and about 1mm long. The resulting conduction heat load is negligible.

TEC Selection

Total Head Loads		
Qactive Qa (W)	1.8	1.8
Qradiation Qr (W)	0.00240	0.00135
Qconvective Qconv (W)	0.00448	0.00448
Qtotal Qtot (W)	*1.8069*	*1.8058*
Temperatures		
TEC hot side (Th)	70	50
TEC cold side (Tc)	17	17
DT(Th-Tc)	53	33
DTmax	64	64
DT/DTmax	0.82813	0.51563
Optimum Q/Qmax	0.15	0.25
Max Q/Qmax	0.18	0.45
Final Results	Max	Min
Head Load/(Optimum Q/Qmax) (W)	***12.05***	***7.22***
Head Load/(Maximum Q/Qmax) (W)	***10.04***	***4.01***

Tab. 1 Thermal characteristic requirements for the choice of the TEC.

Table 1 summarises the values obtained for our component. In particular it can be seen that the temperature difference between hot and cold side is at most DT=53 degrees. A one-stage commercial TEC with a maximum achievable DT_{max} of 64 degrees should be suitable for our package. From the TEC performance diagram we can obtain the optimum and the maximum Q/Qmax values which can be used in selecting the TEC. In Tab. 2 gives the characteristics of the chosen TEC:

Active heat load:	2.0W	
Total heat load:	2.0W	
TEC temperature:	20C (Celsius)	
Maximum Package Temperature: 70C		
Dimensions:		
Length:	10mm (millimiters)	14mm
Width:	10mm	14mm
Height:	2.5mm	3mm
Ceramic substrate:		
Hot side:	AlN	
Cold Side:	AlN	
Internal Construction Solder:	232C SnSb	
Wire Leads:	Au-plated	
External Finishing:		
Hot side:	pretinned ceramic 183C SnPb	
Cold Side:	pretinned ceramic 118C InSn	

Tab. 2 Characteristics of the chosen TEC.

3.3 The fan-out submount

The OXS chip is bonded onto a Si submount with device side up, shown in Fig.4, of dimensions 15x15mm which fits the size of the TEC. We chose not to use flip-chip bonding because of the complicated submount fabrication and the equipment needed to carry out the bonding. The fan-out is first sputter-coated with Ti/Au and then half of it, after photolithography masking process, is etched to provide a large ground pad for bonding the chip and 16 wire bonding pads nearby the chip. These 16 connections are fanned-out towards the two non-fibre coupling edge of the submount allowing bonding to the package feed-through pins. A thermistor holder has been also etched onto the submount to facilitate temperature control. The unetched side of the submount will be used for locating the Si V-grooves carrying the optical fibers. This part of the submount contains V-grooves fabricated prior to Ti/Au deposition for the correct positioning the fibre array as described later.

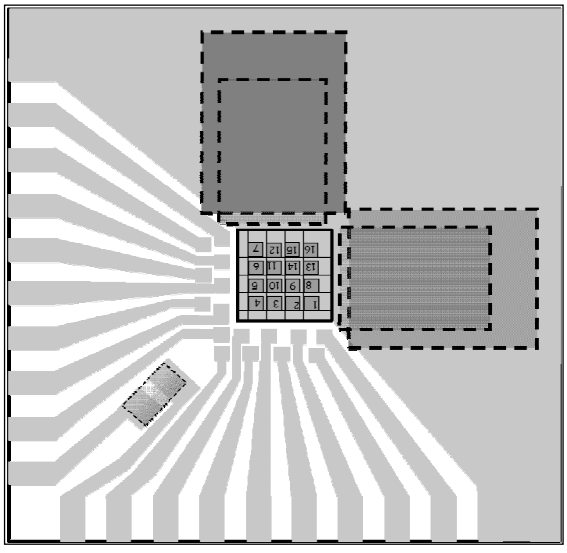


Fig. 4 Fan-Out, Au patterned, holding the 4x4 OXS Matrix (in the centre), two fibers Si V-grooves perpendicular each other (side in dotted lines), and the thermistor .

The chip is bonded on to the fan-out submount using a modified die bonder which allows alignment of chip waveguide features to alignment marks etched into the gold layer of the submount to accuracy within 10μm. AuSn alloy solder perform is used for the die bonding.

3.4 Packaging Assembly and Electrical Connections

The package case has dimensions of 30x30x9 mm (LxDxH) enough to contain all the components. Two sides are used for optical fibre access while the other two for electrical connections. Each of the two adjacent optical faces contains an elongated feed-through window which allows the fibre ribbon access to the chip. This will be sealed by an epoxy filling once the fibre fixation is completed. The package case is machined from CuW alloy, and then sputter-coated with a Ti/Au coating throughout. The other two adjacent sides of the case are each fitted with 10 feed-through pins which includes 8 for OXS electrical connections, one for the ground and one for the thermistor. Furthermore one of the two sides are mounted with two large current capacity feed-through pins for the TEC connections.

The fan-out submount carrying the chip is bonded onto the cold side of the TEC by a high thermal conductivity epoxy, which in turn is also bonded inside the CuW alloy package case in the same manner. A particular wire bonding order is then used in order to connect each single switching cell to the fan-out submount as shown in Fig 5. On the edge of the fan-out submount, double wire bonding is made between the submount and the package feed-through pins to connect th device as well as the thermistor to the outside. The TEC connections are soldered to special allocated large diameter pins able to carry any high current required by the TEC.

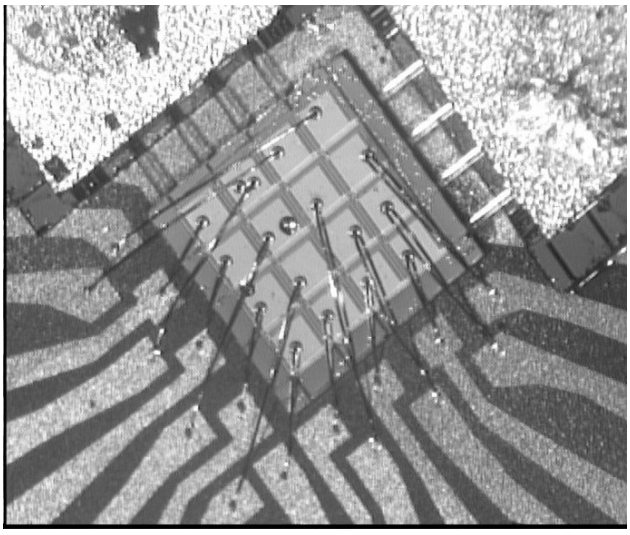


Fig. 5 4x4 OXS Matrix. Wire bonding distribution across the chip and the fan-out.

3.5 Fibre Array Alignment and Fixation

Fibre array alignment and fixation are the two most critical issues in this packaging development. In order to keep the coupling losses to the lowest level achievable, it is very important to ensure the accurate and correct position of the fibre array relative to the chip waveguide ports. It is also vital to design a fixation method that's easy to implement, and at the same time minimizes the potential fibre position drift in the long term.

The most important difference between fibre array coupling and single fibre coupling is that it is usually unrealistic to align multiple fibres individually. Therefore it would be necessary to make a fibre array assembly with fibre ends lying strictly on a straight line. Furthermore, these fibre ends will need to be micro-machined into lenses with proper shape in order to achieve high coupling efficiency. However this method precludes the fabrication of conical lenses. Wedge lenses have to be used instead. This can be relatively easily addressed by including mode expanders are incorporated on the chip to expand spot size up to ~9μm in the horizontal (x) direction in order to match that of a standard single mode fibre, which will also alleviate the horizontal alignment accuracy requirements as well. However in the chips used for package testing this feature is not yet included.

In order to facilitate accurate vertical alignment and limited horizontal adjustment of the fibre array position, a two part Si V-groove design is used to position the fibre array. The horizontal adjustment is necessary because of the limited placement accuracy achievable with our die bonder even when using photolithography-defined alignment marks.

To accommodate potential future upscale of the switch matrix, an 8-fiber Si V-groove carrier piece is designed and fabricated with 250 μm groove pitch. In this packaging process we use every other V-groove to accommodate fibres, giving a 500 μm pitch 4-fibre array matching the 500μm waveguide pitch. Fibre is fixed in the precision Si V-groove carrier first. The entire carrier piece is then mounted onto a linear movement stage on high power laser machining system. The fibre tips are machined by a high power laser beam into wedge shaped fibre lenses with a focal distance of ~9μm. This method ensured that the linearity of the fibre tips are within less than 1μm in the fibre axial (z) direction, and within 0.3μm in the vertical (y) direction.

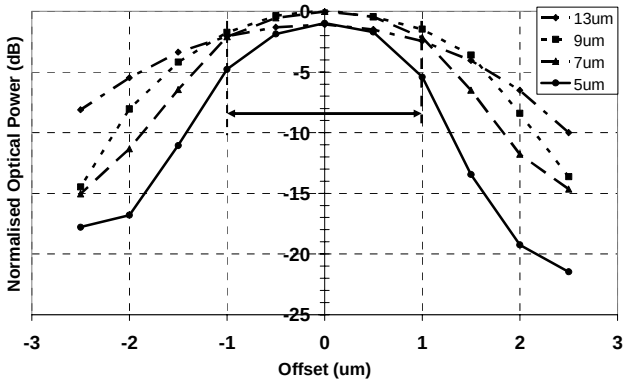


Fig. 6 Optical power as a function of the waveguide offset for 4 different focal lenses.

The focal distance of the wedge lens has been chosen from a selection of different tips tested with the chip. From Fig.9 it

can be seen that only 9 and 13μm tips can achieve a coupling efficiency drop of at most 2 dB within ±1μm vertical alignment error. But 13μm tips have worse peak coupling loss leaving 9μm tip the best solution.

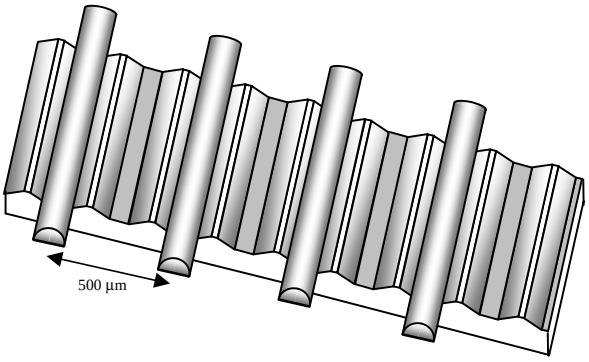


Fig. 7 A schematic of the Si V-groove carrier holding 4-fiber wedge lens array.

Fig.7 illustrates the fabricated Si V-groove carrier holding the fibre lens array. This is then fed through the packaging case and aligned to the chip now situated on the Si submount. Fig.8 illustrates the complicated adjustments that are potentially needed to achieve correct position of the fibre array. These include the following:

- In-plane (x-z plane) rotation: This governs the equal distance between the fibre tip line to the edge of the chip. This distance is importance as the ends of waveguides need to be at the lens focal distance from the fibre tips. As the total length of the base line (distance between the two side fibres) is 750μm and if an allowed axial positioning (i.e., the distance from fibre tip to chip edge) error of ±1μm is allowed, the horizontal in-plane rotational angular error tolerance is only 0.076°.
- Axial rotation (in the x-y plane): This is to ensure that all fibre are aligned to the waveguides vertically at the same time. This is of paramount importance, as the vertical alignment tolerance is in the order of ±0.5 □m if a drop of 1 dB in coupling efficiency is the limit. This rotational angular error therefore needs to be <0.038°.
- Azimuth rotation (in the y-z plane): This is to ensure the beam from the chip enters the fibre at the right angle. This requirement is not critically high. Typically a 1° error can be tolerated.

In addition to these angular adjustments, linear positioning in all three (x, y and z) directions needs to be carried out with the y adjustment being the most critical.

In our design a mechanism of chip positioning is employed to ensure the parallelism between the cleaved chip edge to the submount features, in particular a V-groove positioning system on the submount that matches exactly with inversed V-grooves on the fibre V-groove carrier. Coarse horizontal alignment is achieved by tightly mating the alignment features on the Si V-groove pieces (not shown in Fig.8) with those pre-fabricated on the Si submount. This action would also at the same time ensure that the correct angles are automatically achieved in all rotational movements described above.

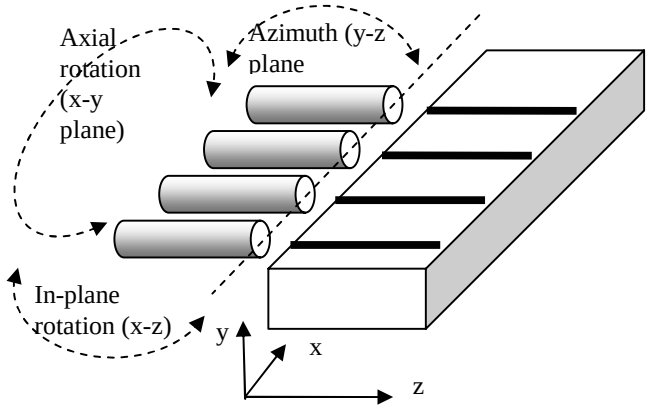
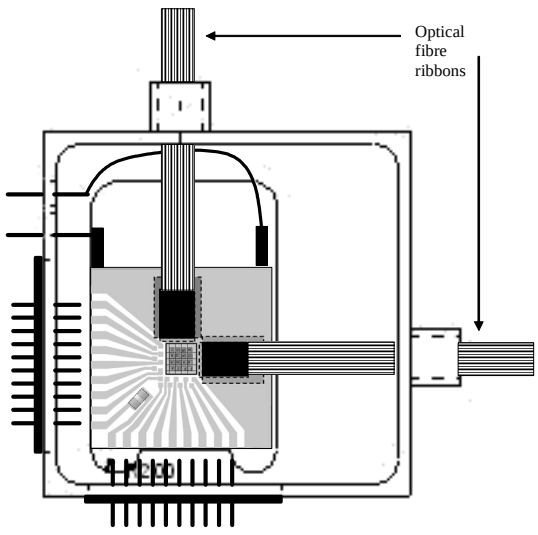


Fig.8 Alignment adjustments needed for correct alignment of fibre array to a chip.

The alignment system is designed so that the fibre centre is lower than the chip edge vertically by ~10 μm when the V-groove carrier is in tight contact with the Si submount. After above mating process that establishes the parallelism, the V-groove fibre array carrier is lifted up and actively aligned to the chip using the spontaneous emission power generated by the chip, which is driven by a pulse generator that applies 1% duty circle pulses alternatively to all 16 switches at 1MHz frequency. The actively alignment involves mostly vertical positioning, although some adjustment needs to be carried out horizontally.

Once the correct position of the fibre array is reached by maximising the output of the fibres, the Si V-groove carrier piece is fixed by dispensing thermally curing adhesive in the narrow gap between the matching V-grooves of the carrier piece and the Si submount. The temperature of the whole package is then raised to cure the epoxy. The fibre ribbon feed-throughs are sealed by an epoxy based filling and the packaged device is finally sealed in dry N_2 ambient with a Kovar lid. Fig.9 illustrates the internal of the finished device and Fig.12 shows a picture of the finished device.



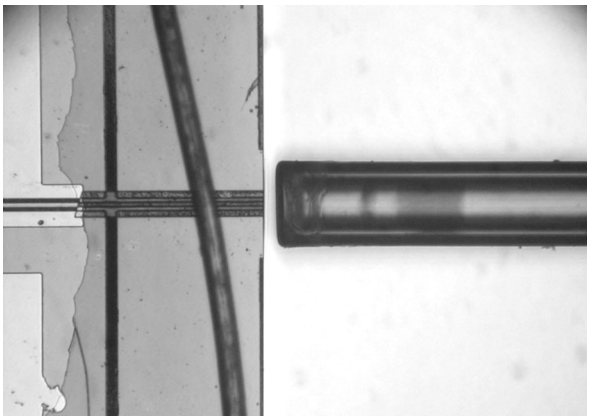


Fig. 9 Schematic illustration of the finished package before sealing (top) and a micro-graph of the fibre lens coupled to the waveguide(bottom).

4 EXPERIMENTAL TEST RESULTS

4.1 Transmission and coupling loss

The packaged devices are tested in terms of their switching performances immediately after the packaging. Fig.11 shows a typical family of 16 transmission curves that are tested after the packaging. At OFF state, all output ports have leakage signal levels that are nearly undetectable (<-70dB) irrespective of whichever input port is used, which is characteristic of the AVC switch's high channel isolation performance. At the switching current of 250mA, the maximum transmission achieved is – 16dB, with the average value at about -21dB and the minimum transmission at about -25dB. The standard deviation is 3.05dB. Comparing this transmission data to the coupling efficiency data measured with the chip prior to the packaging process, it is found that the best case transmission loss (-16dB) is almost entirely due to fibre coupling loss. This loss (8 dB /facet) is consistent with typical values achievable when the laterally unexpanded mode size (~3 μm) is coupled to the wedge fibre lens. This will clearly be reduced in future implementations where an taper mode expander section will be included.

The variation in transmission has contributions form both the performance variation between the switching cells on the chip as well as coupling efficient variations. When the switch cell performance variation of about 3 dB (mainly due to path dependent loss [13]) is deducted from the data, the coupling efficiency variation is about 6 dB between the best and the worst case, or about 3 dB per facet. This is still quite large, and is found to be mainly resulting from the limited linearity and uniformity achieved between the relative y-position of fibre tips. It is often found that each individual fibre can be aligned to achieve higher transmission similar to the best case value, however at the same time other fibres in the array would suffer larger coupling loss. The end results achieved are a compromise to allow reasonable coupling for all ports.

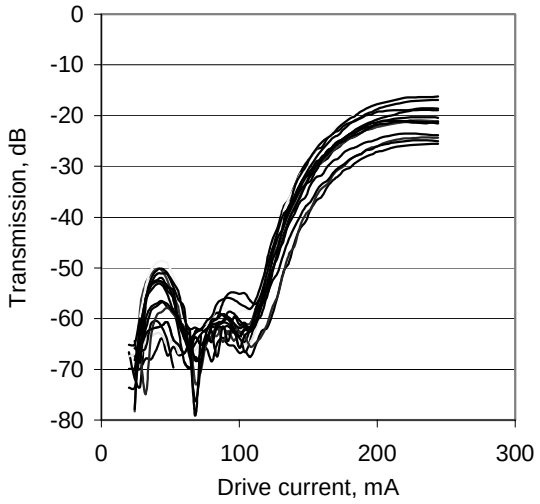


Fig.10 Measured switching characteristics of 16 cells in one switch matrix.

4.2 Back-reflection

The back-reflection of the device after packaging has been measured using a low coherence interferometer which has longitudinal spatial resolution with the device under no injection current.

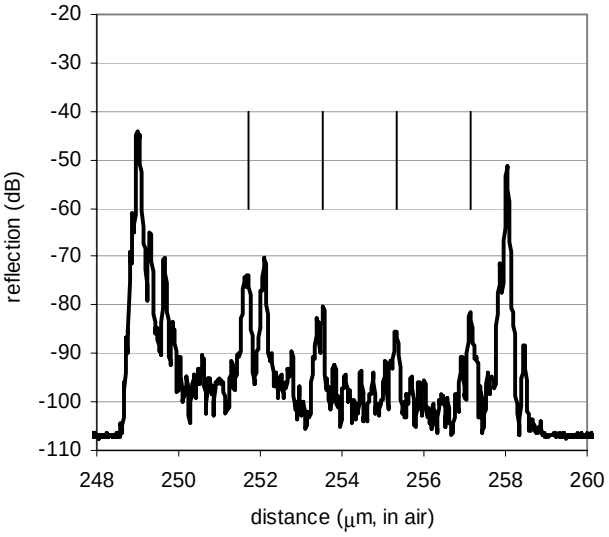


Fig.11 Spatially resolved back-reflection

It can be observed that the highest measured back-reflection level of -45dB results either from the near end fibre tip (uncoated) or the near end facet reflection (which despite AR coating is still in the 10^{-4} region). Due to limited resolution is impossible to distinguish between these two possible reflection sources. A number of very low peaks have been observed (marked by vertical lines in the chart) with a spacing corresponding to the waveguide cross points. These are all below -70 dB. This is proof that passive waveguide perpendicular crossings have sufficiently low scattering levels. Finally the back facet reflection peak can be observed at just under -50dB.

The same measurements have also been carried out with the device under increasing injection current to switch cells in the measured row. No increase in reflection values are observed up to the point when spontaneous emission from the switch device drowns the back reflection signal peaks.

4.3 Long term stability

The packaged devices have been stored in room temperature in a normal laboratory environment for 4 months by the time of this writing. They have also been installed in a switch module with electrical interfaces and subject to continued optical switching experiments in this duration involving the application of switching currents of up to 250 mA. These experiments use temperature control to 20°C provided by the TEC and the thermistor when the thermal load is high (when the duty cycle of the switching operation is high), and sometimes do not use temperature control when the switch operation is sparse. All packaged devices have survived without any obvious deterioration in transmission, which suggests that the fibre fixation method used is stable in such environments.

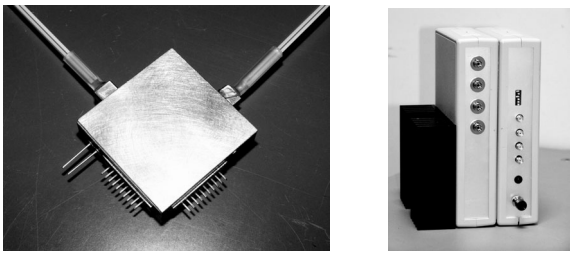


Fig. 12 Packaged optical switch device (left) and a switch module (right).

5 Conclusion and discussion

This paper reports the first attempt to produce a packaged fast 4x4 optical crosspoint switch matrix based on the AVC technology. A packaging process has been carefully designed and implemented. The package design took in consideration thermal management, electrical access, as well as optical fibre coupling and fixation.

The cleaved chip (after AR coating) is bonded to a Si submount using AuSn solder. Relatively large number of electrical connections for a photonic device has been realised using simple wire bonding and the thermal management elements are assembled in the package.

Highly demanding lensed fibre arrays have been fabricated using Si V-groove carrier pieces made in our laboratory. A successful fibre alignment strategy allows the simplified and accurate alignment and stable fixation of the fibre array relative to the switch chip submount assembly which is also made in our laboratory.

The final devices have been tested and demonstrate successful switching operation characteristics with an OFF state leakage of less than -70dB and ON-OFF contrast of >50dB. The finished packages have been used in laboratory optical switching experiments housed in a switch module.

The fibre coupling losses are still relatively high as well as scattered, partly due to the unmatched mode size between the chip and the wedge fibre lens and partly due to the limited precision of fibre array linearity. Both causes can be improved in future fabrications.

Acknowledgment

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